

What is claimed is:

1. 1. A method of forming an inductor, comprising in the order recited:
  2. (a) providing a semiconductor substrate;
  3. (b) forming a dielectric layer on a top surface of said substrate;
  4. (c) forming a lower trench in said dielectric layer;
  5. (d) forming a resist layer on a top surface of said dielectric layer;
  6. (e) forming an upper trench in said resist layer, said upper trench aligned to said lower trench, a bottom of said upper trench open to said lower trench; and
  7. (f) completely filling said lower trench and at least partially filling said upper trench with a conductor in order to form said inductor.
1. 2. The method of claim 1, further including:
  2. forming a via in said dielectric layer to an I/O terminal pad in said substrate.
1. 3. The method of claim 2, further including forming a wirebond pad electrically contacting said I/O terminal pad through said via.
1. 4. The method of claim 2, further including forming a solder ball connection contacting said I/O terminal pad through said via.

1       5. The method of claim 4, wherein said forming said solder ball connection comprises  
2       electroplating one or more metals over said I/O terminal pad.

1       6. The method of claim 1, wherein:

2           step (c) includes forming a via in said dielectric layer, a bottom of said via open to  
3       an I/O terminal pad in said substrate;  
4           step (d) includes forming a trench in said resist layer, said trench aligned to said  
5       via and a bottom of said trench in said resist layer open to said via; and  
6           step (f) includes completely filling said via and at least partially filling said trench  
7       with said conductor to form a raised contact pad.

1       7. The method of claim 6, further including forming a solder ball connection contacting  
2       said raised contact pad.

1       8. The method of claim 7, wherein said forming said solder ball connection comprises  
2       evaporating one or more metals through a mask aligned to said substrate.

1       9. The method of claim 7, wherein said forming said solder ball connection comprises  
2       electroplating one or more metals over said I/O terminal pad.

1 10. The method of claim 1, wherein said lower trench is formed a predetermined distance  
2 into said dielectric layer.

1 11. The method of claim 10, wherein:

2 step (c) includes forming vias to underpass connection wires in said substrate, said  
3 vias formed in a bottom surface of said lower trench; and  
4 step (f) includes completely filling said vias with said conductor.

1 12. The method of claim 1, further including:

2 (g) removing said resist layer and forming a conductive passivation layer over said  
3 inductor.

1 13. The method of claim 1, wherein said upper and lower trenches are spiral trenches.

1 14. The method of claim 1, wherein said conductor comprises Cu or a TaN/Ta liner and a  
2 Cu core.

1 15. A method of forming an inductor, comprising in the order recited:

2 (a) providing a semiconductor substrate;

3 (b) forming a dielectric layer on a top surface of said substrate;

4 (c) forming a lower trench in said dielectric layer;

5 (d) forming a conformal conductive liner in said lower trench and over a top

6 surface of said dielectric layer;

7 (e) forming a conformal Cu seed layer over said conductive liner;

8 (f) forming a resist layer on said substrate;

9 (g) forming an upper trench in said resist layer, said upper trench aligned to said

10 lower trench, a bottom of said upper trench open to said lower trench;

11 (h) electroplating Cu to completely fill said lower trench and at least partially fill

12 said upper trench in order to form said inductor;

13 (i) removing said resist layer;

14 (j) selectively forming a conductive passivation layer over all exposed Cu

15 surfaces; and

16 (k) selectively removing said Cu seed layer from regions of said conductive liner

17 overlying said surface of said dielectric layer and removing said conductive liner from

18 said surface of said dielectric layer.

- 1 16. The method of claim 15:
  - 2 further including after step (e) removing said Cu seed layer from regions of said
  - 3 conductive liner overlying said top surface of said dielectric layer and leaving said seed
  - 4 layer on said conductive liner on sidewalls and a bottom surface of said lower trench; and
  - 5 wherein step (k) does not include removing said seed layer from said regions of
  - 6 said conductive layer overlying said top surface of said dielectric layer.
- 1 17. The method of claim 15, further including:
  - 2 forming a via in said dielectric layer to an I/O terminal pad in said substrate.
- 1 18. The method of claim 17, further including:
  - 2 forming a via in said dielectric layer, said via aligned to said I/O terminal;
  - 3 forming a polyimide layer over said substrate, said polyimide layer aligned to said
  - 4 via in said dielectric layer; and
  - 5 forming a via in said polyimide layer, said via in said polyimide layer aligned to
  - 6 said I/O terminal and defining a wirebond pad.
- 1 19. The method of claim 17, further including forming a solder ball connection contacting
- 2 said I/O terminal pad through said vias in said polyimide layer and said dielectric layer.

1    20. The method of claim 19, wherein said forming said solder ball connection comprises  
2    evaporating or sputtering a pad limiting metallurgy layer and a seed layer and  
3    electroplating a Pb layer or a Pb/Sn alloy layer.

1    21. The method of claim 15, wherein:  
2        step (c) includes forming a via in said dielectric layer to an I/O terminal pad in  
3    said substrate;  
4        step (d) includes forming a conformal conductive liner in said via in said  
5    dielectric layer;  
6        step (g) includes forming a trench in said resist layer, said trench aligned to said  
7    via in said dielectric layer, a bottom of said trench open to said via in said dielectric layer;  
8    and  
9        step (h) includes electroplating Cu to completely fill said via in said dielectric  
10   layer and at least partially fill said trench to form a raised contact pad.

1    22. The method of claim 21, further including forming a solder ball connection contacting  
2    said raised contact pad.

1    23. The method of claim 22, wherein said forming said solder ball connection comprises  
2    evaporating or sputtering a pad limiting metallurgy layer and a Pb layer or a Pb/Sn alloy  
3    layer through a mask aligned to said substrate.

1    24. The method of claim 22, wherein said forming said solder ball connection comprises  
2    sputtering a pad limiting metallurgy layer and a seed layer and electroplating a Pb layer or  
3    a Pb/Sn alloy layer.

1    25. The method of claim 15, wherein said lower trench is formed a predetermined  
2    distance into said dielectric layer.

1    26. The method of claim 25, wherein:  
2        step (c) includes forming vias to underpass connection wires in said substrate, said  
3        vias formed in a bottom surface of said lower trench; and  
4        step (h) includes electroplating Cu to completely fill said vias in said bottom  
5        surface of said lower trench.

1    27. The method of claim 15, wherein said conductive passivation layer comprises a layer  
2    of Ni or a layer of Au over a layer of Ni.

1    28. The method of claim 15, wherein said upper and lower trenches are spiral trenches  
2    and said inductor is a spiral inductor.

1    29. The method of claim 15, wherein said dielectric layer comprises an upper layer of  
2     $\text{Si}_3\text{N}_4$  in contact with a top surface of an  $\text{SiO}_2$  layer, said  $\text{SiO}_2$  layer in contact with a top  
3    surface of a lower  $\text{Si}_3\text{N}_4$  layer.

1    30. The metal of claim 15, wherein step (h) electroplates Cu to a depth of at least 5  
2    microns.

1 31. A semiconductor structure, comprising:  
2       an inductor having a top surface, a bottom surface and sidewalls, a lower portion  
3       of said inductor extending a fixed distance into a dielectric layer formed on a  
4       semiconductor substrate and an upper portion extending above said dielectric layer; and  
5       means to electrically contact said inductor.

1 32. The structure of claim 31 wherein said lower portion of said inductor comprises a  
2       conductive liner and a core conductor and said upper portion of said inductor comprises  
3       said core conductor.

1 33. The structure of claim 32, wherein said core conductor is Cu and said liner comprises  
2       a dual layer of TaN and Ta.

1 34. The structure of claim 32, wherein said upper portion further comprises a conductive  
2       passivation layer on a top surface and sidewalls of said upper portion of said inductor.

1 35. The structure of claim 34, wherein said passivation layer comprises a layer of Ni or a  
2       layer of Au over a layer of Ni.

1 36. The structure of claim 31, wherein said inductor has a height defined by said sidewalls  
2       of greater than about 5 microns.

1    37. The structure of claim 31, wherein said lower portion extends a distance of less than 3  
2    microns into said dielectric layer.

1    38. The structure of claim 31, wherein said means for contacting said inductor includes  
2    integral vias extending from said bottom of said inductor through said dielectric layer and  
3    electrically contacting pass through metallurgy in said substrate.

1    39. The structure of claim 38, wherein said top surface of said inductor over said vias is  
2    closer to a top surface of said dielectric layer than portions of said top surface of said  
3    inductor not over said vias.

1    40. The structure of claim 31, wherein said inductor extends parallel to a top surface of  
2    said dielectric layer in a spiral coil.

1    41. The structure of claim 40, wherein said inductor is about 2 to 30 microns wide and  
2    adjacent coils of said spiral coil are spaced apart about 2 to 20 microns.

1    42. The structure of claim 31, wherein said inductor has an inductance of greater than  
2    about 0.5 nH.

1 43. The structure of claim 31, wherein said inductor has a Q factor of greater than about  
2 25.

1 44. The structure of claim 31, wherein said inductor has a Q factor of greater than about  
2 40.

1 45. The structure of claim 31, further including a contact pad comprising a via formed in  
2 said dielectric layer, said via exposing at least a portion of an I/O terminal pad in said  
3 substrate, sidewalls of said via and at least a portion of said I/O terminal pad covered with  
4 a passivation layer over a conformal seed layer over a conductive liner.

1 46. The structure of claim 45, wherein said conductive liner comprises a dual layer of  
2 TaN and Ta, said seed layer comprises Cu and said passivation layer comprises a layer of  
3 Ni or a layer of Au over a layer of Ni.

1 47. The structure of claim 46, further including an Al or Au wire conductively bonded to  
2 said contact pad.

1 48. The structure of claim 46 further including a layer of pad limiting metallurgy on said  
2 passivation layer and a solder ball on said pad limiting metallurgy.

1    49. The structure of claim 48, wherein said pad limiting metallurgy comprises one or  
2    more layers selected from the group consisting of Cr layers, CrCu layers, Au layers, Cu  
3    layers and TiW layers and said solder ball comprises Pb or Pb/Sn alloy.

1    50. The structure of claim 45, wherein said top surface of said inductor is in a different  
2    plane than a top surface of said contact pad.

1    51. The structure of claim 45, wherein a top surface of said inductor is higher than said  
2    top surface of said contact pad relative to a top surface of said dielectric layer.

1    52. The structure of claim 31, further including:  
2                an I/O terminal pad formed in said substrate; and  
3                a raised contact pad in electrical contact with said I/O terminal pad, said raised  
4    contact pad having a top surface, a bottom surface and sidewalls, a lower portion of said  
5    inductor extending said fixed distance into said dielectric layer formed on a  
6    semiconductor substrate and an upper portion extending above said dielectric layer.

1    53. The structure of claim 52, wherein said lower portion of said raised contact pad  
2    comprises a conductive liner and a core conductor and said upper portion of said raised  
3    contact pad comprises said core conductor.

1 54. The structure of claim 53, wherein said core conductor is Cu and said liner comprises  
2 a dual layer of TaN and Ta.

1 55. The structure of claim 53, wherein said upper portion further comprises a conductive  
2 passivation layer on said top surface and sidewalls of said upper portion of said raised  
3 contact pad.

1 56. The structure of claim 55, wherein said passivation layer comprises layer of Ni or a  
2 layer of Au over a layer of Ni.

1 57. The structure of claim 56, further including an Al or Au wire conductively bonded to  
2 said raised contact pad

1 58. The structure of claim 56 further including a layer of pad limiting metallurgy on said  
2 passivation layer and a solder ball on said pad limiting metallurgy.

1 59. The structure of claim 58, wherein said pad limiting metallurgy comprises one or  
2 more layers selected from the group consisting of Cr layers, CrCu layers, Au layers, Cu  
3 layers and TiW layers and said solder ball comprises Pb or Pb/Sn alloy.

1    60. The structure of claim 52, wherein said top surface of said inductor is in a different  
2    plane than a top surface of said raised contact pad.

1    61. The structure of claim 52, wherein a top surface of said inductor is higher than said  
2    top surface of said raised contact pad relative to a top surface of said dielectric layer.